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SEMESTER 1, 2021/2022

CSCI 3301 CAAL Section 03

COMPUTER ARCHITECTURE AND ASSEMBLY LANGUAGE

**Lab 2**

**PREPARED BY:**

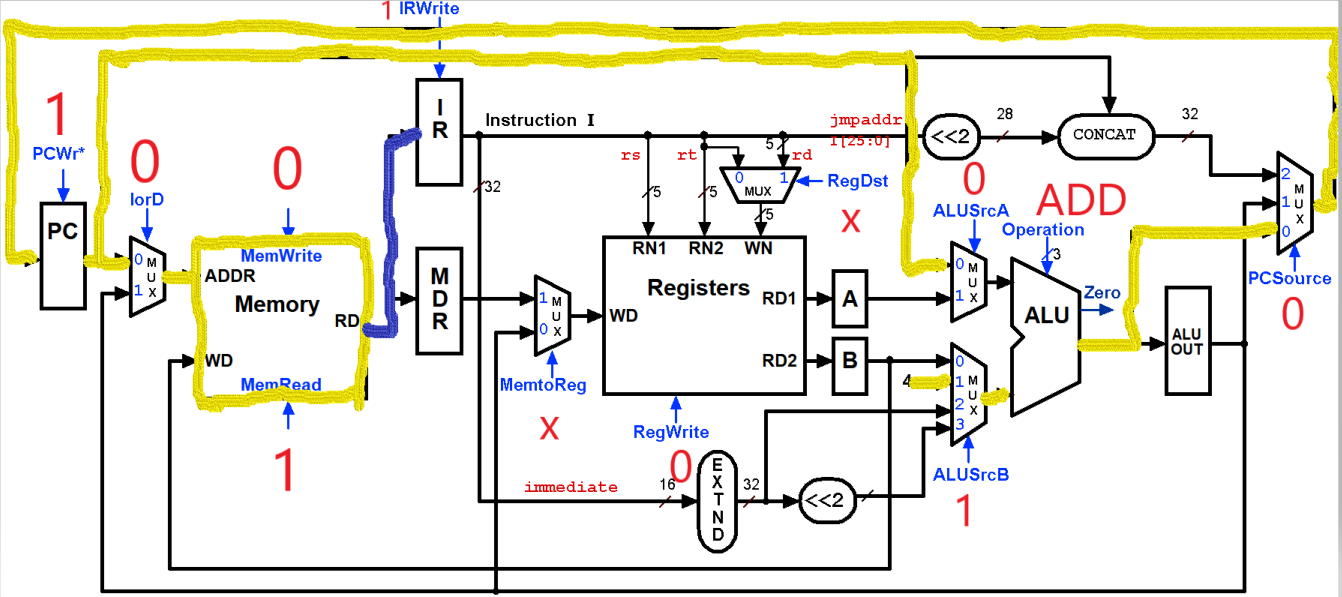
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1. Figure 1. xori instruction during Instruction fetch (IF) cycle.

PC = PC + 4

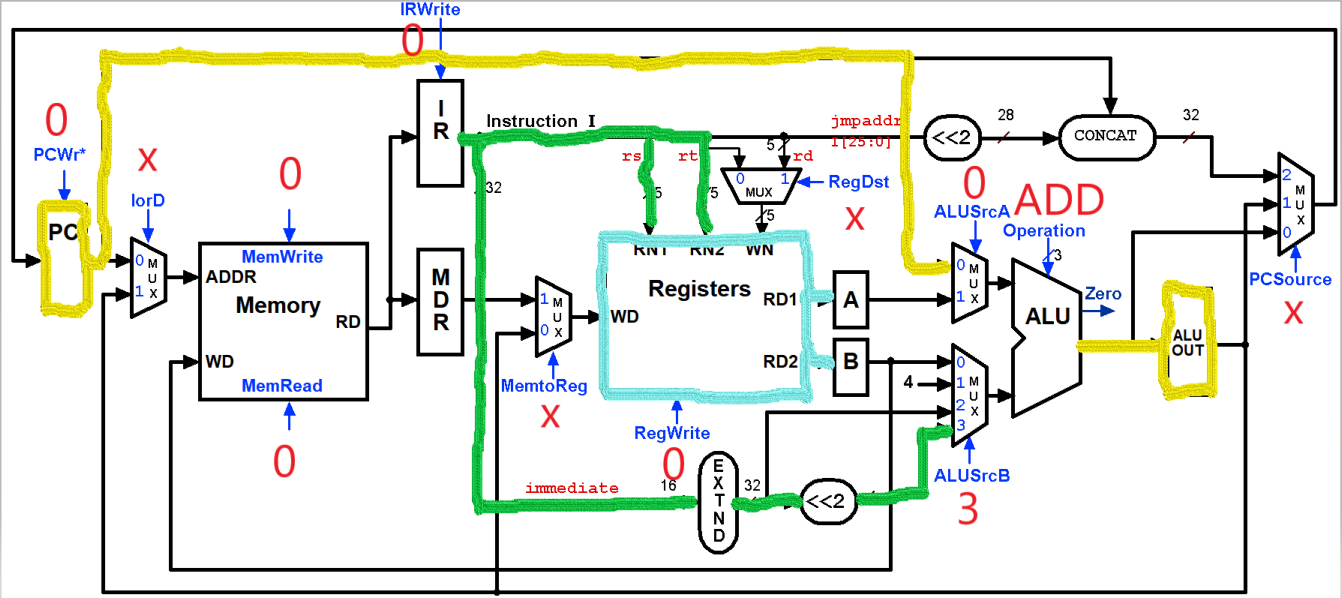


1. Figure 2. add instruction during Instruction decode (ID) cycle.

A = REG [ IR [ 25 - 21 ] ]

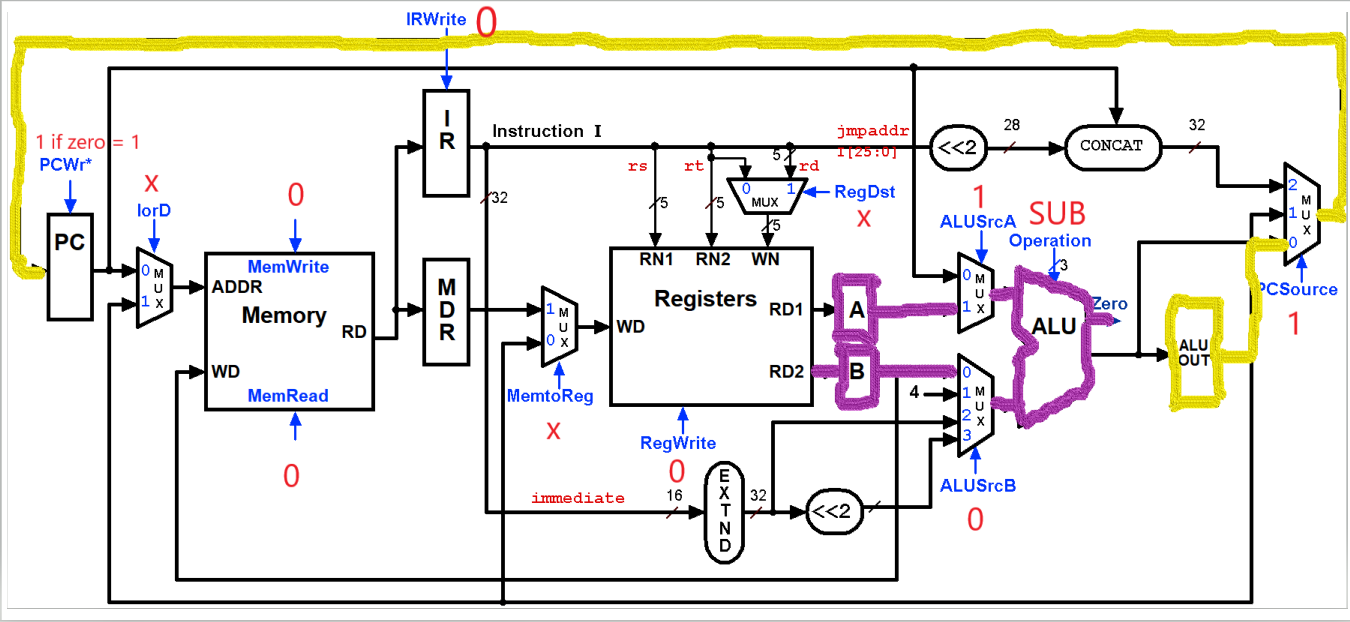
A = REG [ IR [ 20 - 16 ] ]

ALUOut = PC + (signe-extend (IR [15 - 0 ]) << 2 )



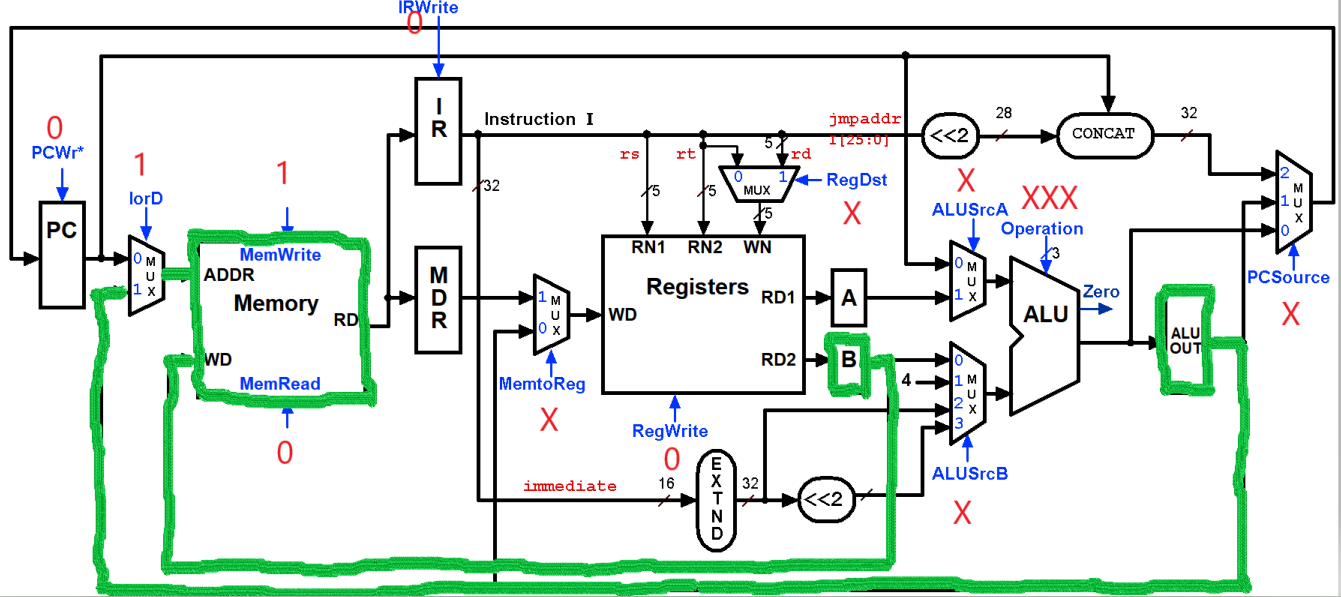
1. Figure 3. beq instruction during Execution (EX) cycle.

If ( A == B) then PC = ALUOut



1. Figure 4. sw instruction during Memory access (MEM) cycle.

Memory [ ALUOut ] = B



1. Figure 5. lw instruction during memory read completion (WB) cycle.

Reg [ IR [ 20 - 16 ] ] = MDR

